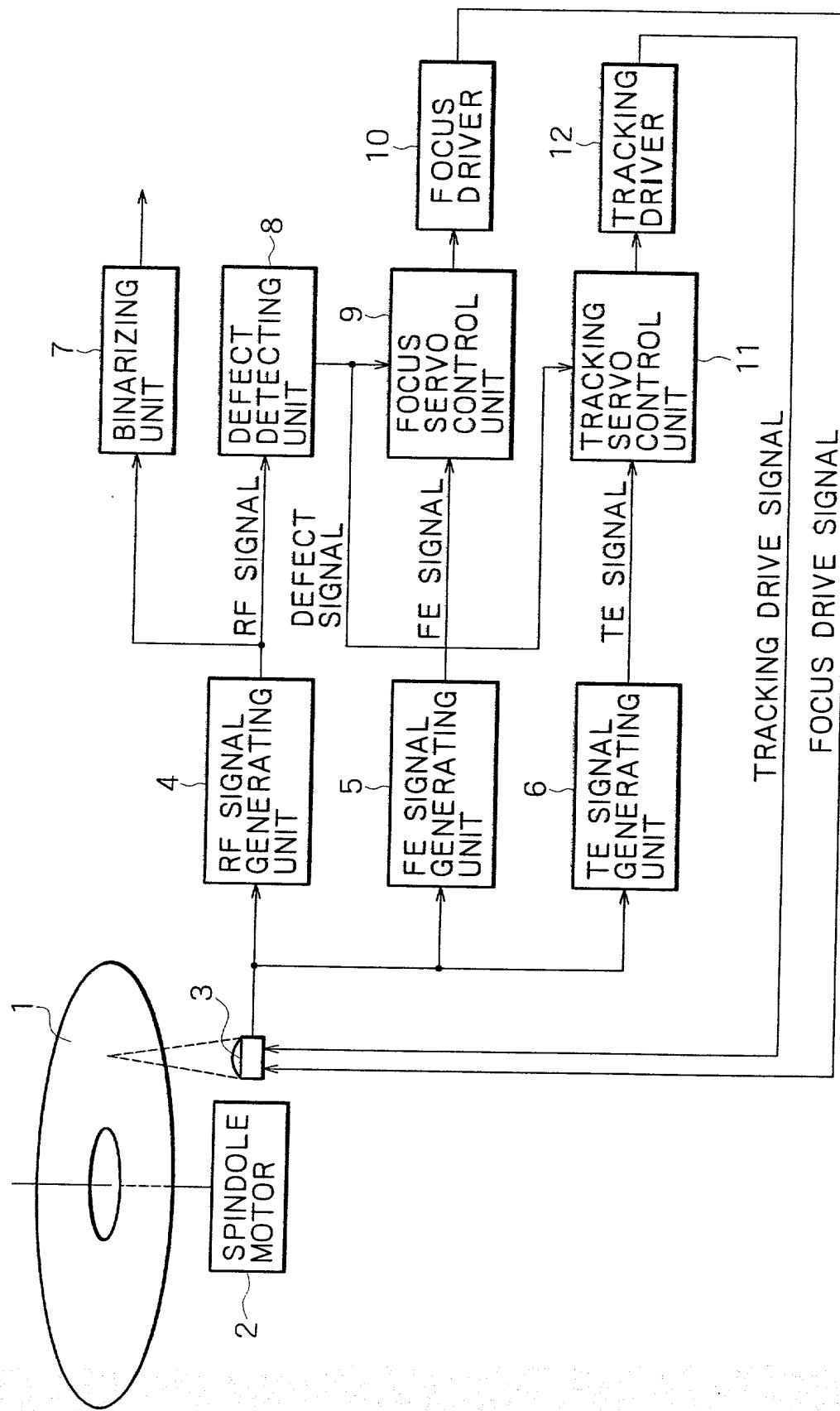


FIG. 1



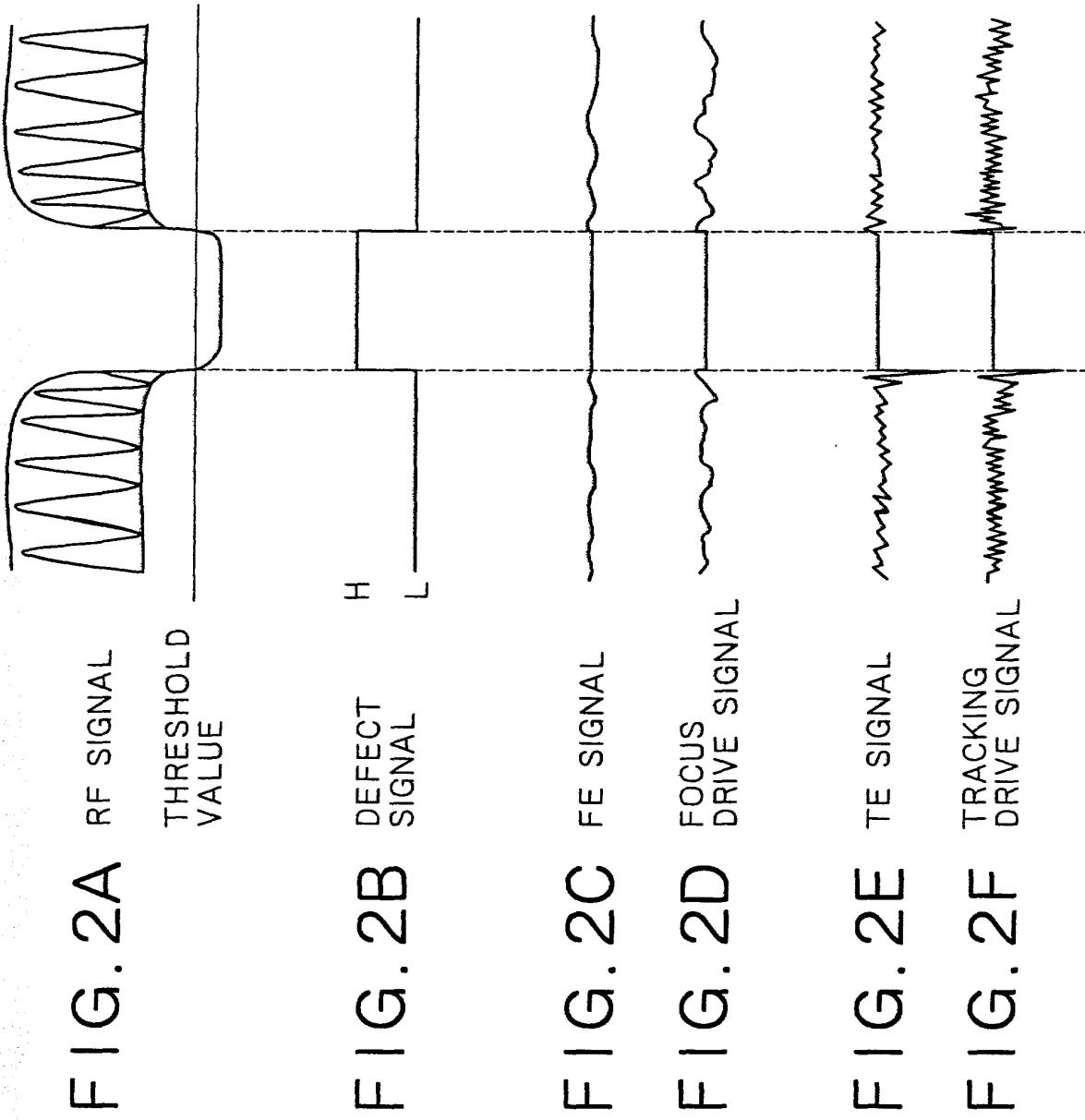


FIG. 3A

DEFECT  
SIGNAL



FIG. 3B

FE SIGNAL



FIG. 3C

FOCUS  
DRIVE SIGNAL



FIG. 3D

TE SIGNAL



FIG. 3E

TRACKING  
DRIVE SIGNAL

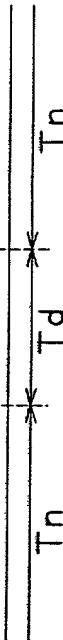


FIG. 4

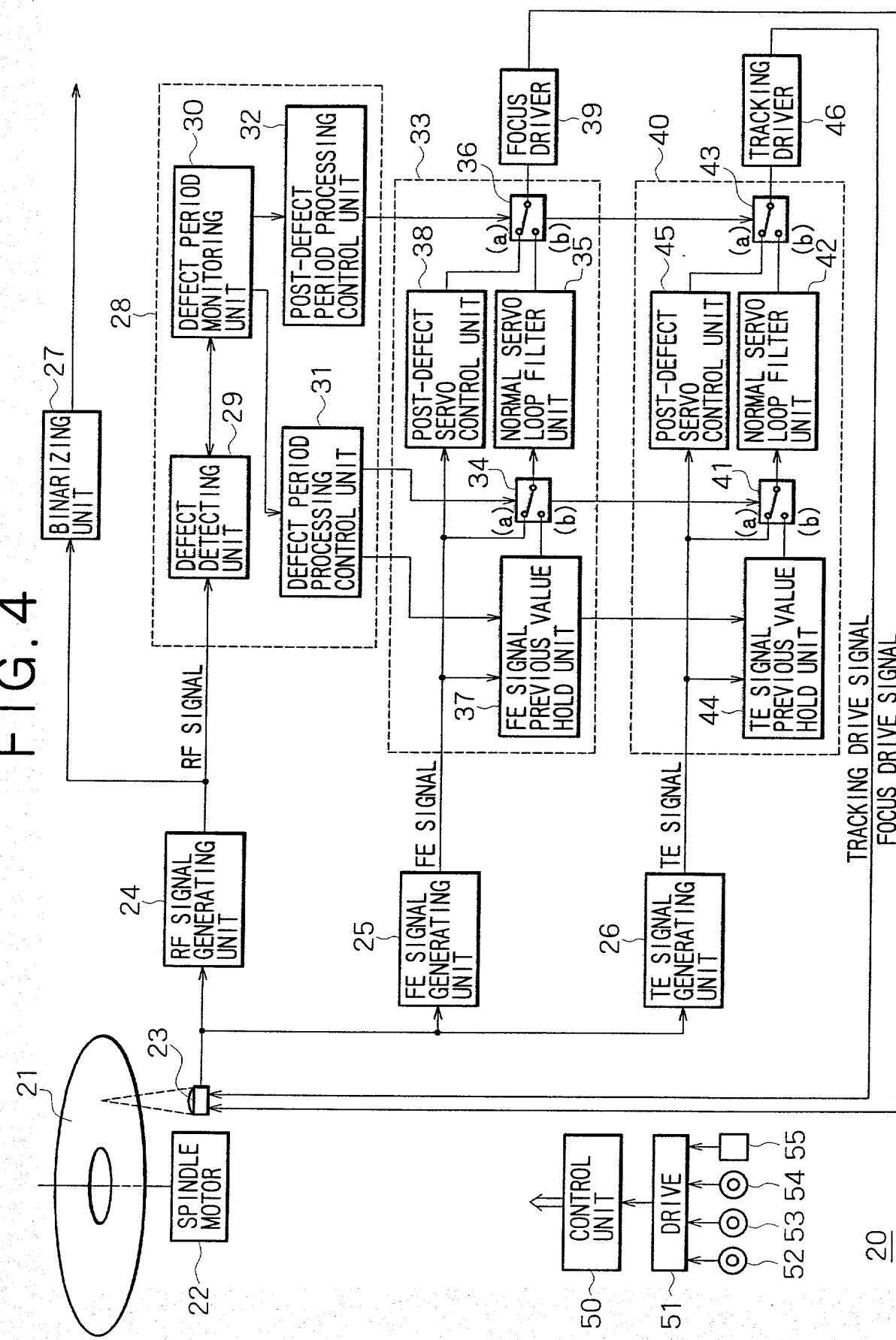
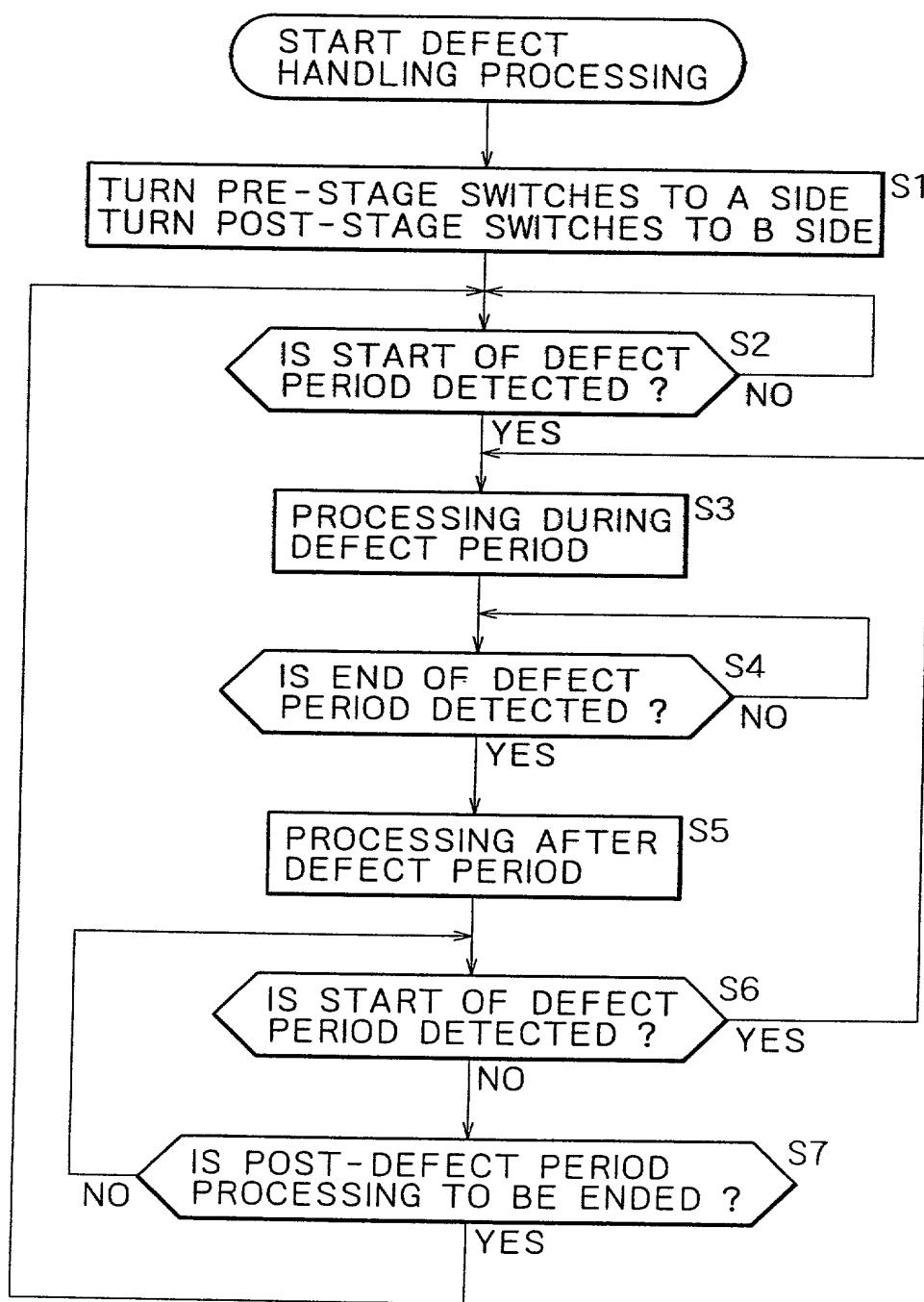


FIG.5



10002226 141201

FIG. 6A

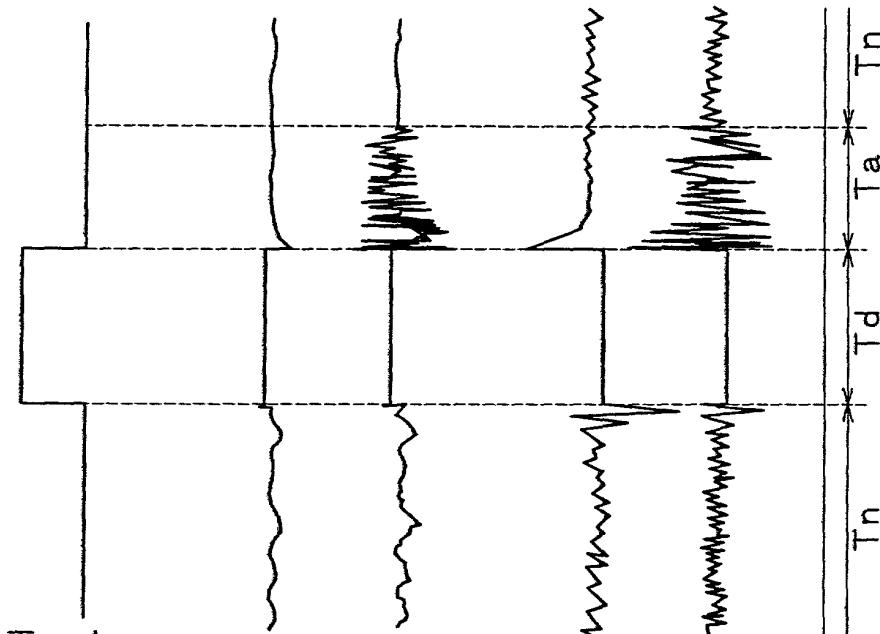


FIG. 6B

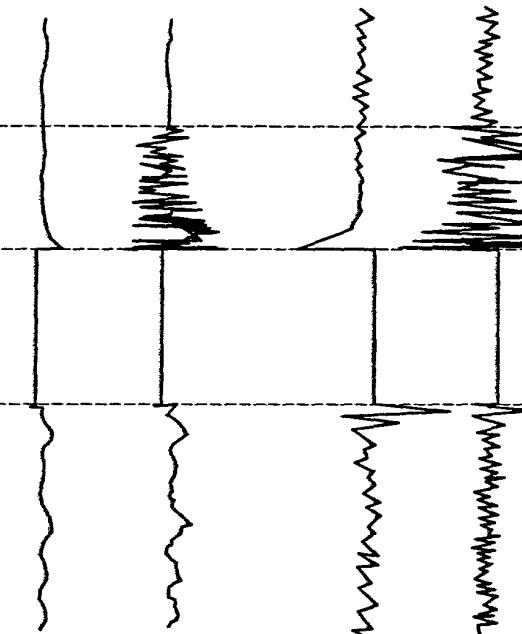


FIG. 6C

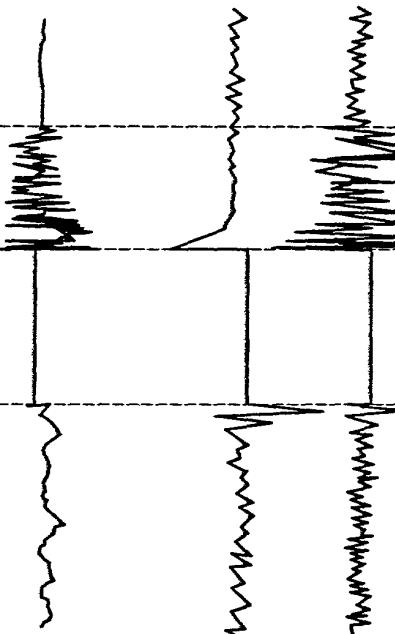


FIG. 6D

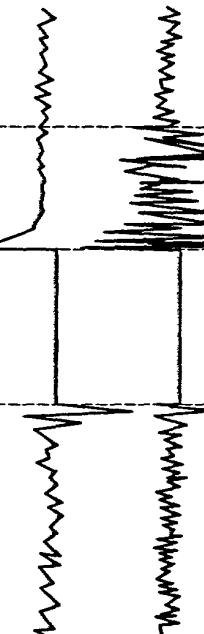


FIG. 6E



FIG. 7A

DEFECT  
SIGNAL

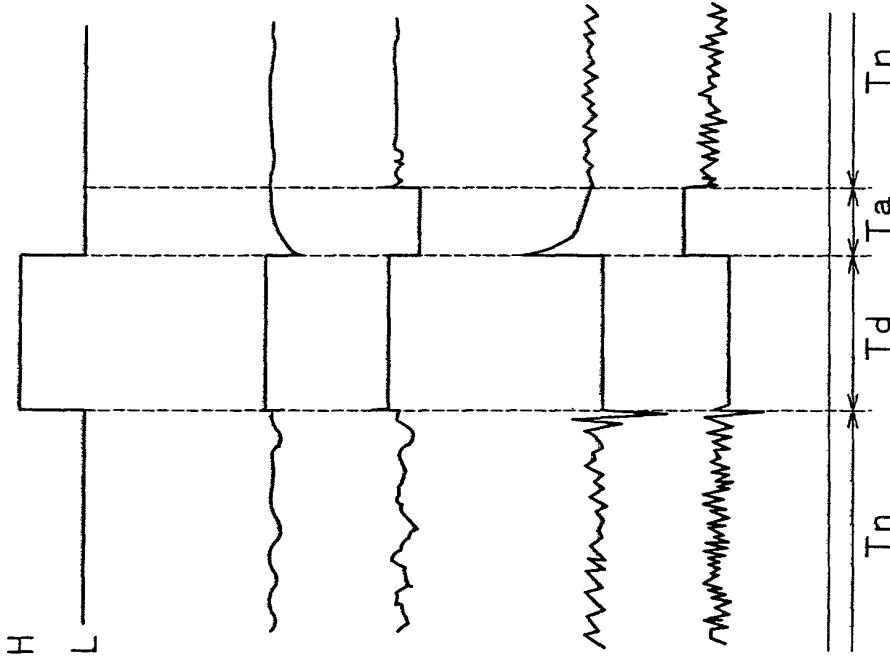


FIG. 7B

FE SIGNAL

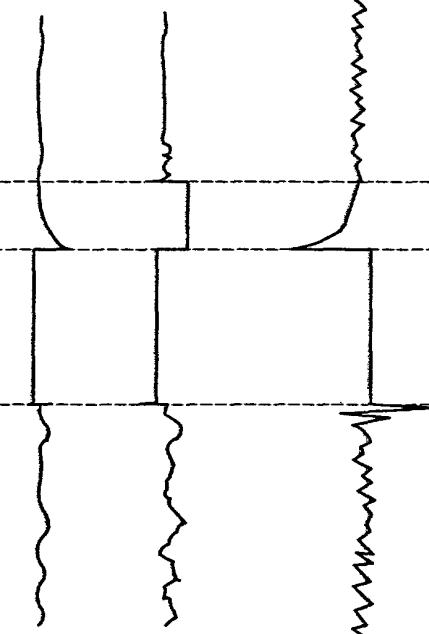


FIG. 7C

FOCUS  
DRIVE SIGNAL

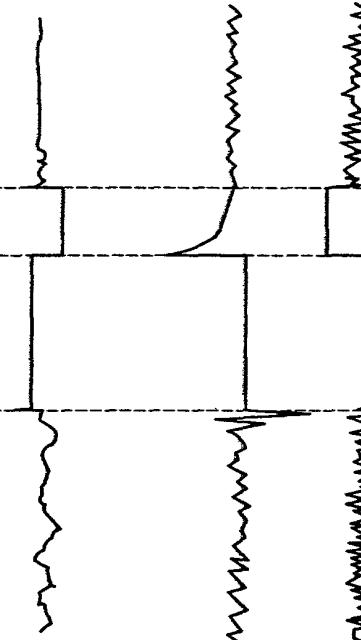


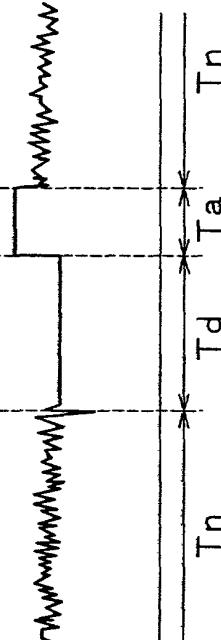
FIG. 7D

TE SIGNAL



FIG. 7E

TRACKING  
DRIVE SIGNAL



$T_n$   $T_d$   $T_a$   $T_n$

# FIG. 8. FET GATED CIRCUIT

FIG. 8A

DEFECT  
SIGNAL

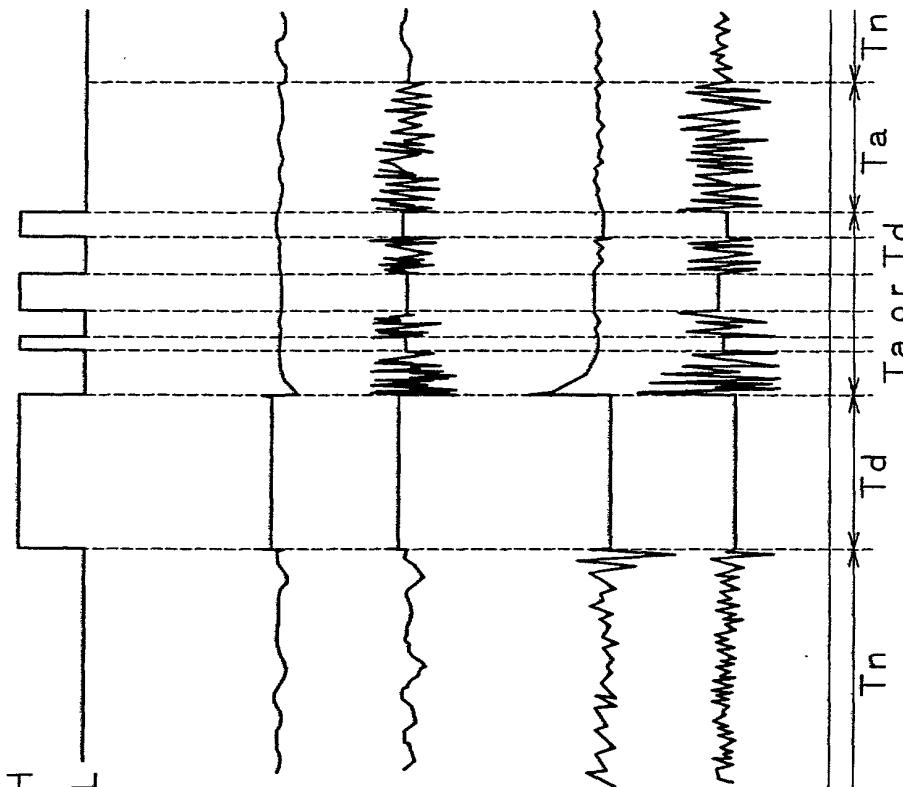


FIG. 8B

FE SIGNAL

FIG. 8C

FOCUS  
DRIVE SIGNAL

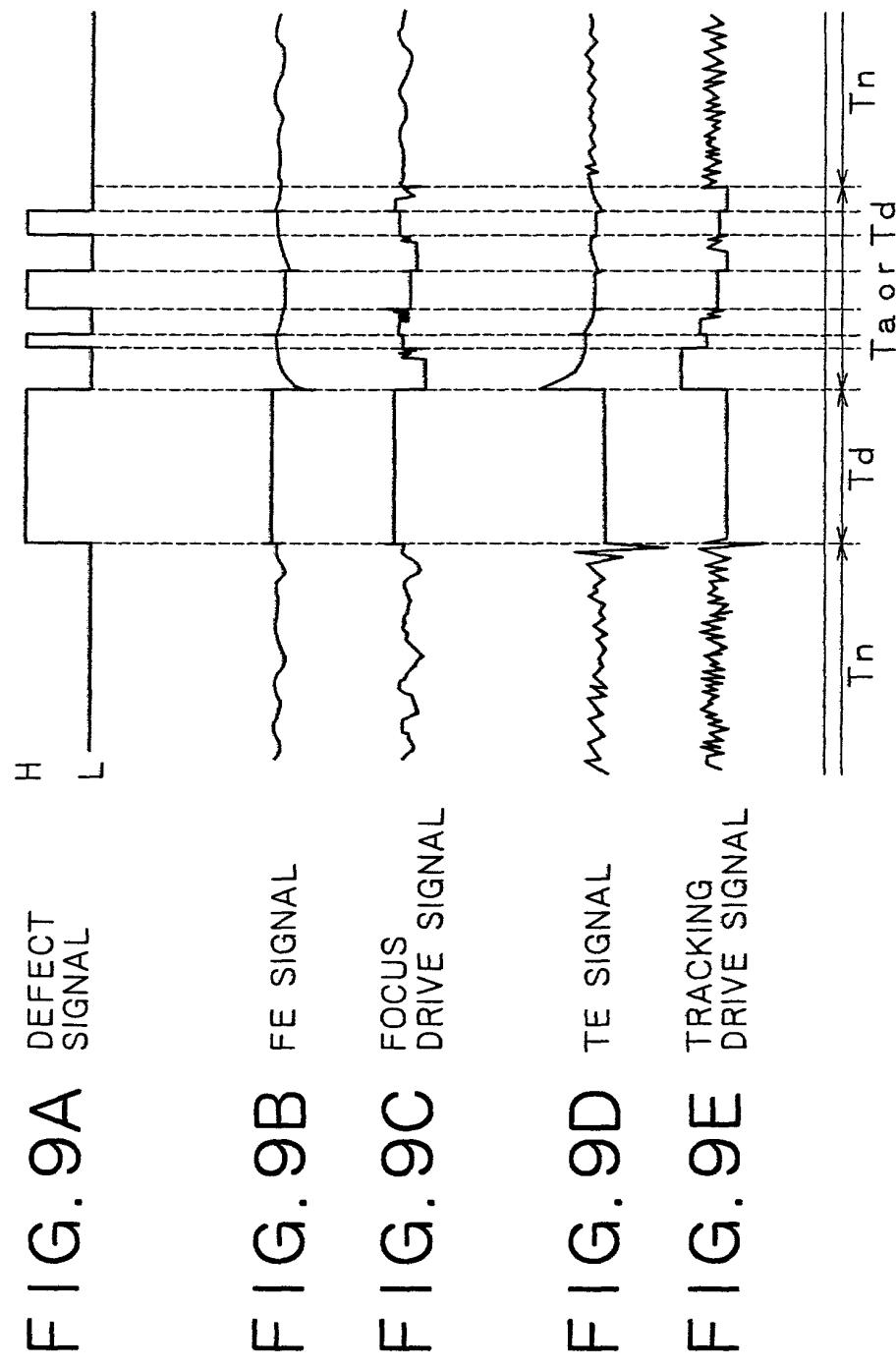
FIG. 8D

TE SIGNAL

FIG. 8E

TRACKING  
DRIVE SIGNAL

FIGURE 9. Sequence



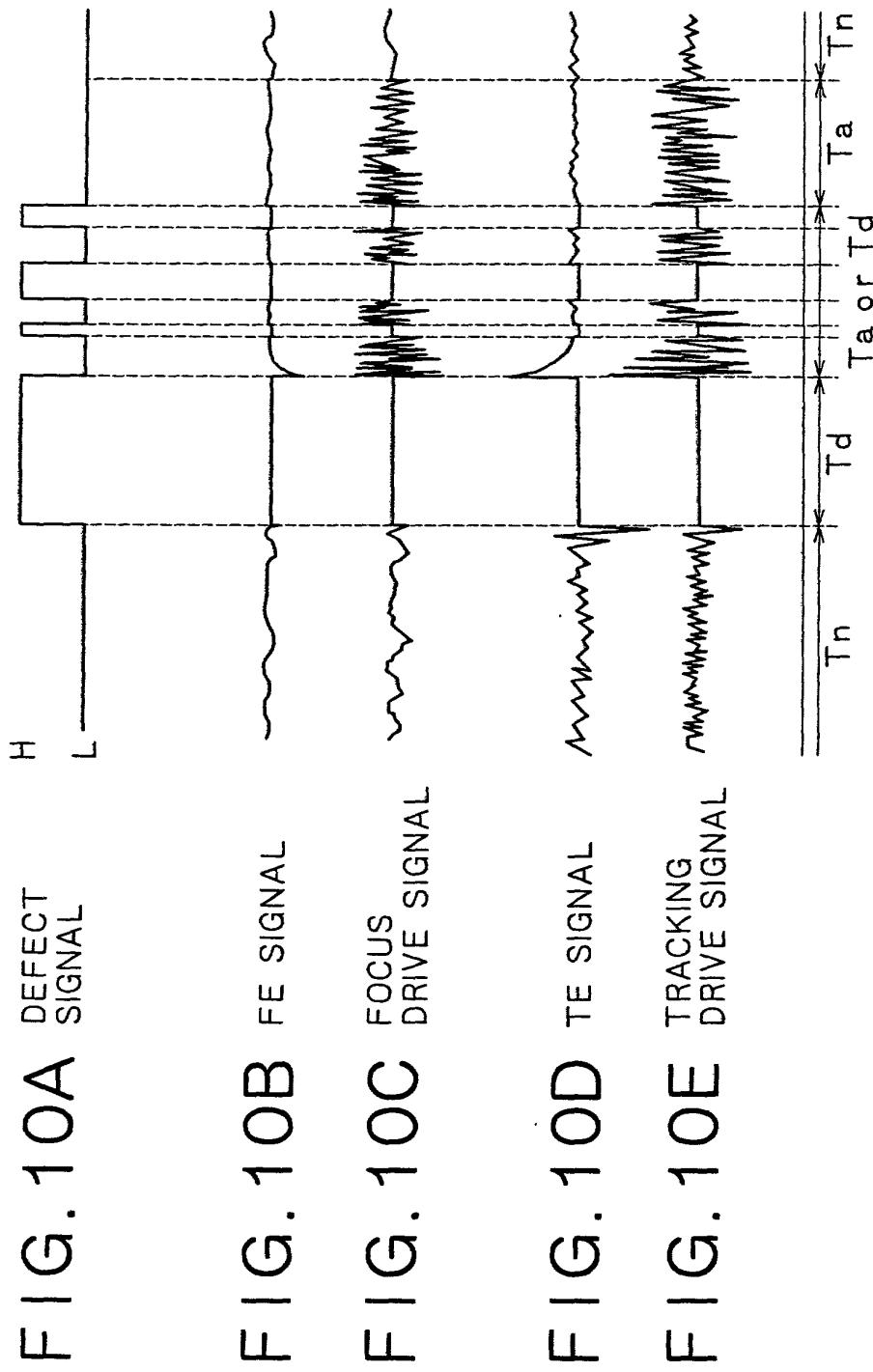


FIG. 11A DEFECT SIGNAL

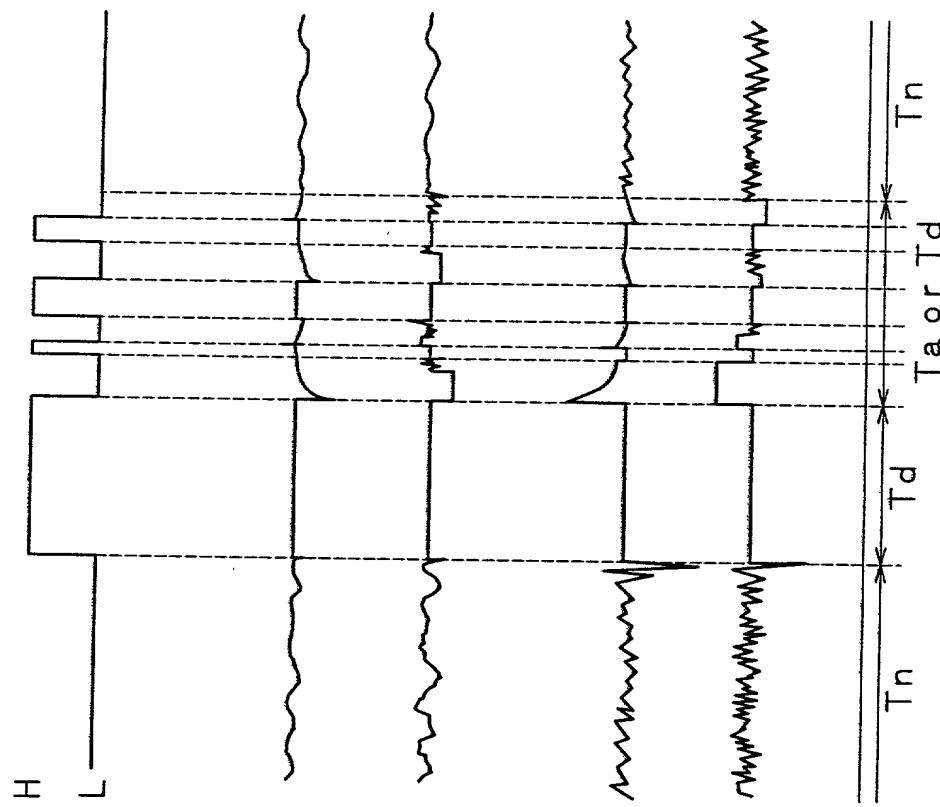


FIG. 11B FE SIGNAL

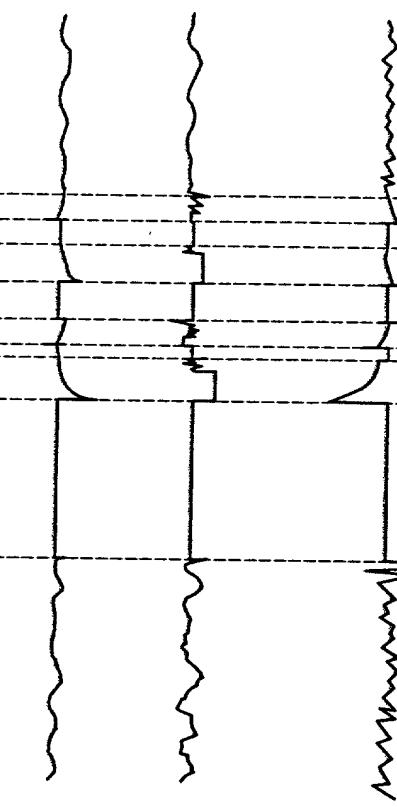


FIG. 11C FOCUS DRIVE SIGNAL

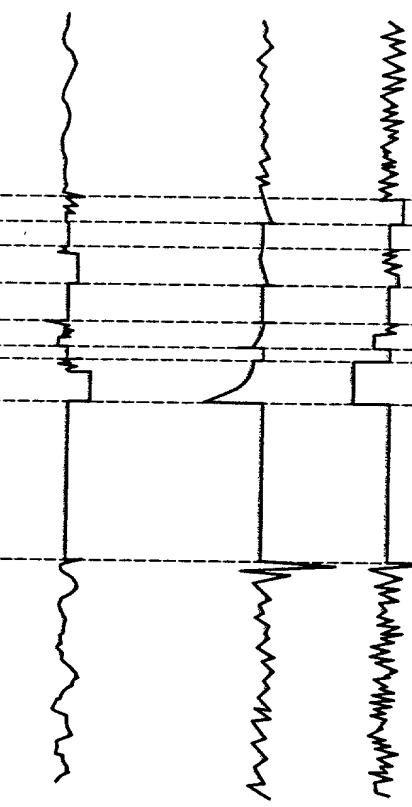


FIG. 11D TE SIGNAL

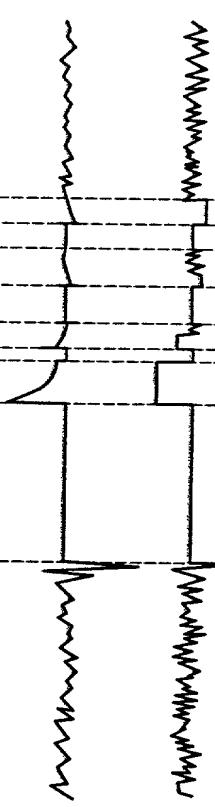


FIG. 11E TRACKING DRIVE SIGNAL